should be withdrawn (M.P.E.P. §706.07(c) and (d)). In the Response filed on October 24, 2002, Applicants amended claim 1-5, 7, 9-14, 16-19, 21, and 31-33 to address the 35 U.S.C §112, second paragraph, rejections contained in the non-final Office Action of May 24, 2002. This amendment did not change the scope of the claims substantively examined. Therefore, because substantive rejections made in the Office Action of May 24, 2002 were not maintained (Applicants' argument thereto are deemed moot by the Examiner) and new grounds of rejections were introduced in the Office Action of January 8, 2003, the new grounds of rejection are not necessitated by the amendment and Applicants should be given a chance to respond to the Office Action's new grounds of rejection. Therefore, the finality of the Office Action is premature and should be withdrawn.

Drawings

Five sheets of drawings were filed initially with this application. However, the Office Action does not indicate whether these drawings are acceptable. Applicants respectfully request the indication of acceptability during the next official communication from the U.S. Patent and Trademark Office.

Specification

The Office Action objects to the specification and requests that 1) at numerous lines and pages of the specification, a "space" be inserted between words, and 2) throughout the specification, all "circuitry layer" be changed to "circuit layer."

With respect to the request to insert a "space" at the various locations, Applicants respectfully submit that, after reviewing the electronic version of the specification, spaces are already provided at all lines and pages specified by the Office Action. The "spaces" are uneven between words at different lines of the specification because the entire specification is "full justified." Therefore, inserting "spaces" in locations specified by the Office Action will inevitably create smaller spaces in other lines. Moreover, attempts to compensate for this could disrupt the Tables in the specification. Therefore, Applicants respectfully ask that this objection be withdrawn.

With respect to the request to change "circuitry layer" to "circuit layer," Applicants respectfully submit that the terms "circuitry layer" and "circuit layer" are both well accepted terms in the art. One of ordinary skill in the art will easily understand that the two terms are interchangeable. Therefore, the change is unnecessary and the objection should be withdrawn.

With respect to both of the foregoing objections, Applicants respectfully request the withdrawal thereof especially in view of the burden and expense that would be placed on Applicants in attempting to change the specification as requested, and especially when no actual inaccuracies or errors are present.

Summary of Amendments

The specification is amended to correct a typographical error recommended by the

Office Action.

Claims 1, 9, and 17 are amended to more particularly claim the subjection matter of the invention. Support for these amendment can be found in the last paragraph of page 12 of the specification. Therefore, no new matter is introduced.

Claims 4 and 13 are canceled and their subject matter are added to claims 1, 9 and 17.

Summary of the Office Action

Claims 1-2, 4-11, 13-18, 21-24 are rejected under 35 U.S.C. §103(a) as being unpatentable over by U.S. Patent No. 6,294,744 ("KINOSHITA") in view of U.S. Patent No. 5,208,656 ("MATSUYAMA").

Regarding claims 1-2, 5, 8-11, 14, 18, 21, 24, the Office Action alleges that KINOSHITA discloses all recitations except that it does not disclose or teach a thickness of the conductor circuitry layer less than a half of the viahole diameter and less than 25 micrometers. To cure this deficiency, the Office Action relies on MATSUYAMA which discloses a wiring layer of 4 micrometers (Col 4, line 64) and a through-hole diameter of between 50 to 70 micrometers (Col 6, line 8). The Office Action then concludes that modifying KINOSHITA to arrive at the presently claimed invention is obvious if KINOSHITA is combined with MATSUYAMA. The Office Action alleges that the motivation for such combination is to provide an improvement of a finer ultra circuit

pattern on the printed wiring board.

Regarding claims 4, 13, 17, the Office Action admits that KINOSHITA does not disclose the conductor circuit layer having a roughened surface but alleges that MATSUYAMA teaches the conductive layer which is roughened. Therefore the Office Action concludes that the combination of the two documents to result in the recited roughened surface would have been obvious in order to achieve bonding laminated layers of the multi-layered wiring board.

Regarding claims 6, 15, and 22, the Office Action alleges that MATSUYAMA teaches a wiring board having an interlaminar insulative resin layer made of thermoplastic resin and concludes that it would have been obvious to modify KINOSHITA to use thermoplastic resin in order to provide excellent heat resistance, and small thermal expansion coefficient.

Regarding claims 7, 16, 23, the Office Action alleges that MATSUYAMA teaches a ratio between a viahole diameter and an interlaminar insulative resin layer thickness being within a range of 1 to 4. The Office Action then concludes that it would have been obvious to modify KINOSHITA with MATSUYAMA's ratio in order to prevent damaging electrical reliability of the wiring board.

Claims 3, 12, 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,294,744 ("KINOSHITA") in view of U.S. Patent No. 5,208,656

("MATSUYAMA") and further in view of U.S. Patent No. 5,509,200 ("FRANKENY").

The Office alleges that the combination of KINOSHITA and MATSUYAMA would disclose all recitations of claims 3, 12, and 19 except the recitation "the plating layer surface being roughened." The Office Action then alleges that FRANKENY shows a plating layer (12) having a roughened surface disclosed in its figures 7, 9-12. The Office Action concludes that it would have been obvious to combine all three documents in order to provide a reliable electrical connection, seal a boundary and bind two or more stackable layers into the multi-layered circuit board.

Claims 25-28, and 31 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,294,744 ("KINOSHITA") in view of U.S. Patent No. 4,769,270 ("NAGAMATSU").

The Office Action alleges that KINOSHITA discloses all claim recitations except for "an interlaminar insulative layer being formed of a composite of fluroresin and heat-resistant thermoplastic resin." The Office Action then alleges that NAGAMATSU's interlaminar insulative layer is formed of a composite of fluororesin fiber cloth and heat-resistant thermoplastic resin and that the cloth comprises voids which are impregnated with thermosetting resin. The Office Action concludes that it would have been obvious to use NAGAMATSU's interlaminar insulative layer in KINOSHITA in order to improve electro-conductivity and provide thermal-expansion or contraction rates between materials

constituting the wiring board.

Claims 32-33 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,294,744 ("KINOSHITA") in view of U.S. Patent No. 4,769,270 ("NAGAMATSU"), and further in view of U.S. Patent No. 5,208,656 ("MATSUYAMA").

The Office Action alleges that the combination of KINOSHITA and NAGAMATSU teaches all the recitations of claims 32-33 except for "the a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4" and "the conductor circuit layer has a thickness less than 25 μm." But the Office Action alleges that MATSUYAMA, as discussed above, discloses these missing recitations and concludes that one would combine all three documents in order to prevent damaging electrical reliability of the wiring board.

Claim 29 is rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,294,744 ("KINOSHITA") in view of U.S. Patent No. 4,769,270 ("NAGAMATSU"), and further in view of U.S. Patent No. 5,509,200 ("FRANKENY").

The Office Action alleges that KINOSHITA and NAGAMATSU teach all the recitations of claim 29 except that they do not disclose that the plating layer is roughened. The Examiner then relied on FRANKENY to allege that it has a roughened surface disclosed in Figures 7, 9-12.

Response to Rejections

With respect to rejections of claims 1-2, 4-11, 13-18, and 21-24 under 35 U.S.C. §103(a) as being unpatentable over KINOSHITA in view of MATSUYAMA, it is well settled that in order to establish a prima facie case of obviousness, the combination of the cited documents must disclose all recitations of the rejected claims. Here, the combination of the two cited documents would not teach, disclose, or suggest all recitations of the amended independent claims 1, 9, and 17. Specifically, none of the cited documents discloses that "at least one of the surfaces of the conductor circuits is roughened to a depth of 1 to 10 μm."

Even if the combination were to teach all the recitations of the claimed invention, as the Examiner is fully aware, in order to make a proper combination, there must be some suggestion or motivation in the documents to make such combination. Here, there is no suggestion in either documents to arrive at the recitation that "at least one of the surfaces of the conductor circuits is roughened to a depth of 1 to 10 μm."

Therefore, the rejections of claims 1-2, 4-11, 13-18, 21-24 under 35 U.S.C. §103(a) is improper and should be withdrawn.

With respect to the rejections of claims 3, 12, 19 under 35 U.S.C. §103(a) as being unpatentable over KINOSHITA in view of MATSUYAMA and further in view of FRANKENY, Applicants respectfully submit that the rejections are improper and should

be withdrawn.

First, the Examiner is mistaken in alleging that FRANKENY shows a plating layer (12) having a roughened surface disclosed in its figures 7, 9-12. In fact, layer 12 of figures 7, 9-12 of FRANKENY does not disclose a roughened surface.

Second, even disregarding the mis-reading of FRANKENY, the combination of these three cited document would still NOT disclose, teach, or suggest ALL the recitation of the amended claims. Specifically, the combination of these three cited documents would not teach that "at least one of the surfaces of the conductor circuits is roughened to a depth of 1 to 10 μm."

Even if the combination were to teach all the recitations of the claimed invention and the Examiner's reading of FRANKENY were accurate, as the Examiner is fully aware, in order to make a proper combination, there must be some suggestion or motivation in the documents to make such combination. Here, there is no suggestion in either documents to arrive at the recitation that "at least one of the surfaces of the conductor circuits is roughened to a depth of 1 to 10 μm."

With respect to the rejections of claims 25-28, and 31 under 35 U.S.C. §103(a) as being unpatentable over KINOSHITA in view of NAGAMATSU, Applicants respectfully submit that the rejection is improper and should be withdrawn.

Applicants respectfully submit that NAGAMATSU does not cure the difficiency of

KINOSHITA in several aspects: A) contrary to the recited composite of fluororesin fiber cloth and thermoplastic resin, NAGAMATSU's inorganic fiber cloth (layer 4) is distinct from the thermoplastic resin layer 3; B) the Office Action's alleged "motivation" to combine the two documents not found in any of the two documents and has no connection with the presently claimed recitation that the interlaminar insulative resin is a composite of fluororesin and heat-resistant thermoplatic resin, composite of fluroresin and thermosetting resin, or a composite of thermosetting resin and heat-resistant thermoplastic resin. Therefore, the rejection is improper and should be withdrawn.

With respect to rejections of claims 32-33 under 35 U.S.C. §103(a) as being unpatentable over KINOSHITA in view of NAGAMATSU, and further in view of MATSUYAMA, Applicants again submit that the rejection is improper and should be withdrawn.

Since claims 32 and 33 are dependent from claim 25, claims 32 and 33 contain all recitations of claim 25. As discussed above, NAGAMATSU does not cure the difficiency of KINOSHITA. Contrary to the recited composite of fluororesin fiber cloth and thermoplastic resin, NAGAMATSU's inorganic fiber cloth (layer 4) is distinct from the thermoplastic resin layer 3. Therefore, the rejection is improper and should be withdrawn.

With respect to the rejection of claim 29 under 35 U.S.C. §103(a) as being unpatentable over KINOSHITA in view of NAGAMATSU, and further in view of

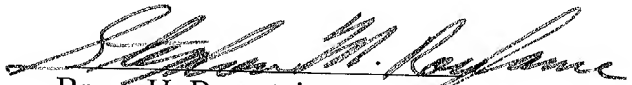
FRANKENY, the rejection is again improper and should be withdrawn.

Since claim 29 is dependent from claim 25, claim 29 contains all recitations of claim 25. As discussed above, NAGAMATSU does not cure the difficiency of KINOSHITA. Contrary to recited the composite of fluororesin fiber cloth and thermoplastic resin, NAGAMATSU's inorganic fiber cloth (layer 4) is distinct from the thermoplastic resin layer 3. Also, the Examiner's understanding of FRANKENY is mistaken. Contrary to the Examiner's allegation, layer 12 of figures 7, 9-12 of FRANKENY does not disclose a roughened surface. Therefore, the combination of the all these cited documents would not arrive at all recitations of claim 29 and therefore the rejection is improper and should be withdrawn.

CONCLUSION

In view of the foregoing, it is believed that all of the claims in this application are in condition for allowance, which action is respectfully requested. If any issues yet remain which can be resolved by a telephone conference, the Examiner is respectfully invited to telephone the undersigned at the telephone number below.

Respectfully submitted,
Seiji SHIRAI et al.



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Appendix A: Marked up copy of the specification amendment.

For the paragraph bridging page 1 and page 2 of the specification:

The multilayer printed wiring board having the filled viahole structure is however disadvantageous in that a surface portion of the plating metal exposed outside the hole for viahole (the surface will be referred to as "viahole surface" henceforth) is easily depressible. If an interlaminar [rein insulating] insulative resin layer is formed on a conductor circuitry layer irrespectively of such a depression existent on the viahole surface, a corresponding depression will develop on the surface of the interlaminar insulative resin layer, and cause the plating metal film to break and also a trouble in mounting electronic parts on the wiring board.

Appendix B: Marked up copy of the claim amendments.

1. A multilayer printed wiring board comprising conductor circuit layers each having a respective thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes having an inner wall filled with a plating layer having a surface to form a viahole having a diameter[,] ; wherein:

the surface of said plating layer [extending] extends out of the through-holes and [lying] lies in a substantially same level as the surface of the conductor circuit layer disposed in the interlaminar insulative resin layer in which the plating layer also lies;

at least one of the surfaces of the conductor circuits is roughened to a depth of 1 to 10 μm; and

the thickness of said conductor circuit layer [being] is less than a half of the viahole diameter.

9. A multilayer printed wiring board comprising conductor circuit layers each having a respective thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes having an inner wall filled with a plating layer having at least one surface to form a viahole having a diameter, wherein the thickness of said conductor circuit layer is

less than a half of the viahole diameter and less than 25 μm and wherein at least one of the surfaces of the conductor circuits is roughened to a depth of 1 to 10 μm.

17. A multilayer printed wiring board comprising conductor circuit layers each with at least one surface wherein at least one of the surfaces of the conductor circuit layer is roughened to a depth of 1 to 10 μm and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes, having an inner wall wherein the inner wall is roughened, filled with a plating layer to form a viahole, wherein:

said roughened inner wall is covered with a roughened electroless plating layer; and

an inner space of said through-hole defined by the electroless plating layer and is filled with an electroplating layer.